

L Number	Hits	Search Text	DB	Time stamp
4	20029	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die)))	USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:26
5	3061	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))	USPAT; US-PGPUB; EPO; JPO USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:27
6	1759	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:28
7	1620	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate carrier (circuit adj board))	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:28
8	1507	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate (circuit adj board)) and (wire wiring)	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:28
9	541	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate (circuit adj board)) and (wire wiring)) and tab	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:29
10	497	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate (circuit adj board)) and (wire wiring)) and tab and lead	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:30
11	436	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate (circuit adj board)) and (wire wiring)) and tab and lead) and (encapsulating encapsulant encapsulated sealing)	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:30
12	263	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate (circuit adj board)) and (wire wiring)) and tab) and lead) and (encapsulating encapsulant encapsulated sealing)) and (solder near1 (bump ball))	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:31
13	259	((chip adj1 chip) (lead adj1 chip) (stacked with (chip die))) and (wire lead wiring) and (second near (chip die semiconductor))) and adhesive) and (substrate (circuit adj board)) and (wire wiring)) and tab) and lead) and (encapsulating encapsulant encapsulated sealing)) and (solder near1 (bump ball))) and (method process)	USPAT; US-PGPUB; EPO; JPO	2004/06/28 08:32